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Strongly asymmetric single-electron transistor operating as zero-biased electrometer

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We have studied a strongly asymmetric Al single-electron transistor with $R_1 \ll R_2$ and $C_1 \gg C_2$, where $R_{1,2}$ and $C_{1,2}$ are the tunnel resistances and capacitances of the first and second junction respectively. Due to asymmetry in its electric parameters, leading to strong asymmetry of the nonlinear I-V curve at zero bias ($V = 0$), the transistor demonstrated remarkable current response to *ac* signal at the values of gate charge Q_0 close to $(n + 1/2)e$, where n is integer. A rather delicate regime of the transistor operation ($V \ll e/C_\Sigma$) being important for unperturbed measurements was examined. The measured curves are in good agreement with a model based on the orthodox theory of single electron tunneling. This specific zero bias regime of asymmetric transistor opens new opportunities for single-electron transistor as ultra-sensitive charge/field sensor.

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Introduction. The single-electron tunneling (SET) transistor is a device consisting of two small tunnel junctions connected in series. Due to close location of these junctions they form a small common electrode (island) which is equipped with a capacitively coupled gate electrode [1]. Due to remarkable correlation of SET events in these junctions, governed by the Coulomb blockade effect, the current through the transistor periodically (period is equal to elementary charge e) depends on the charge induced on its island, so the SET transistor can be used as an extremely sensitive electrometer (see, e.g., Refs. [1, 2]). Due to requirement of high yield in their manufacture, the metallic SET transistors are usually fabricated with tunnel junctions having almost equal areas, so the transistors are nominally symmetric.

Recently, some useful features of asymmetric SET transistors were found experimentally by Weis et al. [3] and Walliser [4], who modelled the behavior of such transistors by numerical methods. One of these useful features is the possibility for asymmetric transistor to operate as a sensitive electrometer even without any *dc* voltage bias when a current response is generated by *ac* or *noise* signal. In this paper we applied a special technique for fabrication of strongly asymmetric SET transistors [5] allowing formation of the transistor junctions not only with different areas, but also with different transparencies of their barriers. Using this technology we fabricated and measured an asymmetric $Al/AlO_x/Al$ SET transistor in the regimes of small *dc* and *ac* bias which are important for delicate measurements. We modelled the transistor behavior applying the orthodox theory of SET [6]. Some of the transistor characteristics are expressed in a simple analytical form, while others are calculated numerically and presented graphically.

1. Sample fabrication. The Al structures (Fig.1) were fabricated on a Si substrate buffered by a sputtered 200 nm thick AlO_x layer. The traditional shadow evap-

Fig.1. Asymmetric Al SET transistor manufactured by the three angle shadow evaporation technique. (a) Top view: arrangement of the metallic layers forming the bottom electrode (grey), island (light grey) and top counter-electrode (white); (b) SEM microphotograph of the transistor structure

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oration technique and e-beam lithography were used in the fabrication process. The suspended mask was used to perform *in-situ* three successive depositions of Al at different angles: first for the bottom electrode, second for the island and third for the counter-electrode. Two oxidation processes were performed in between to form tunnel barriers (see for details Ref. [5]). The design of the structures was nearly the same as developed earlier for the stacked SET transistors which demonstrated very low noise of background charge [5]. In this paper the efforts were focused on study of operation characteristics of a device with strongly unequal junctions. Since the junctions were formed at different fabrication steps, the effect of shrinking the orifices and slits in the mask after each evaporation step resulted in a reduction of area of the second (top) tunnel junction, as shown in Fig.1a.

2. Results and discussion. All measurements were carried out in a dilution refrigerator at temperature $T_{\rm bath} = 25\,$mK. Magnetic field of 1 T was applied to the sample in order to suppress superconductivity in Al electrodes of the transistor. The parameters of the transistor were evaluated as follows: $R_1 = 60\,\text{k}\Omega$, $R_2 = 0.6\,\text{M}\Omega$, $C_1 = 0.26\,$fF and $C_2 = 0.03\,$fF. Its I-V curve is shown in Fig.2. In this strongly asymmetric sample ($R_1 \ll R_2$ and $C_1 \gg C_2 \gg C_g$, where

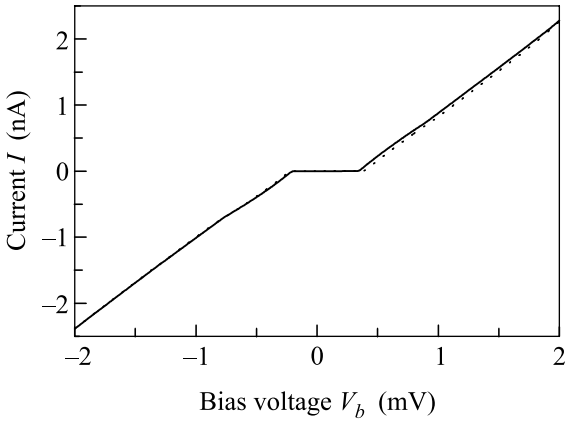

Fig.2. Experimental $I - V$ curve of the studied transistor (solid line) and its theoretical fit with the parameters presented in the text

$C_g = 0.2\,$aF is the gate capacitance) at zero voltage bias and around the gate charge $Q_0 = C_g V_g \approx e/2 + en$ (n is integer and V_g is the gate voltage) we observed the *dc* current response as small antisymmetric peaks. These peaks can be explained by the effect of rectification of the unavoidable voltage noise due to strong asymmetry of the transistor I-V characteristic at $V = 0$ (see also Ref. [3]). Similar behavior of the transistor was observed when an *ac* signal, $V = V_{\rm ac} \sin \omega t$, was applied to the transistor. Moreover, the amplitude of the current peaks strongly depended on the degree of asymmetry (R_2/R_1 and C_1/C_2) and on the amplitude $V_{\rm ac}$ of the *ac* signal. The transistor current response measured in such regime at $V_{\rm ac} = 20\,\mu$V and frequency $\omega/2\pi = 500\,$Hz is shown in Fig.3. Some small discrepancy between experimental and fitted curves in Fig.3 can be explained by

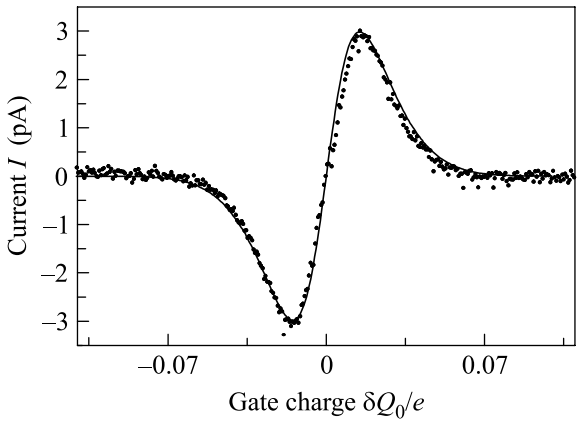

Fig.3. Experimental (points) response curve of the asymmetric SET transistor at harmonic voltage bias with amplitude $V_{\rm ac} = 20\,\mu$V. The fitting curve (solid line) was calculated for the experimentally evaluated parameters of the transistor and the signal amplitude of 23 μV. Effective electron temperature T was assumed to be 40 mK

the presence of the nonzero voltage noise applied to the transistor. It means that in the experimental case we measure the total action of applied *ac* and noise signals, the noise effective level $V_{\rm noise}$ can be estimated to be about of 10 μV. Analogous measured and calculated responses in *dc* voltage bias regime for studied transistor at the same value of Q_0 are shown in Fig.4.

To fit the experimental curve for not very fast *ac* signals ($\omega \ll I/e$, where I is SET current) we applied the orthodox theory of SET [6]. Presenting the gate charge Q_0 in the form $Q_0 = e/2 + en + \delta Q_0$, we expressed appropriate tunneling rates $\Gamma_i^{\pm}$ through the ith junction in positive (+) and negative (−) direction as

$$\Gamma_i^{+} = \frac{k_B T}{e^2 R_i} \frac{\gamma_i}{e^{\gamma_i} - 1}, \quad \Gamma_i^{-} = e^{\gamma_i} \Gamma_i^{+}, \quad i = 1 \text{ and } 2,$$

where

$$\gamma_{1,2} = \frac{e}{C_\Sigma k_B T} (\delta Q_0 \mp C_{2,1} V_{\rm ac} \sin \omega t),$$

and $C_\Sigma = C_1 + C_2 + C_g$, the total capacitance of the island.

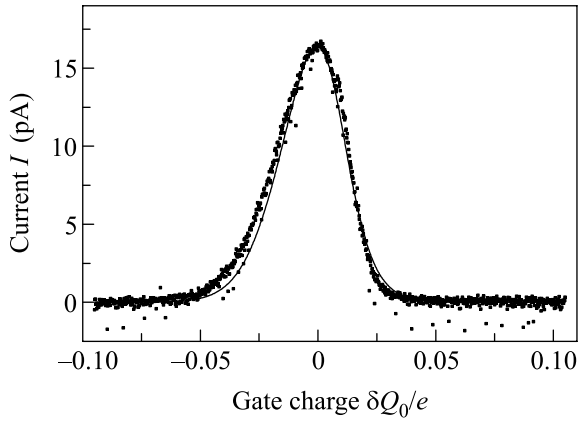

Fig.4. Experimental (points) and calculated (solid line) modulation curves of the asymmetric SET transistor in *dc* bias regime at $V_{\rm dc} = 20\,\mu$V

The SET current across the transistor in the two-charge-state approximation, applicable in our case of not very large signals, is expressed as (see, e.g., Ref. [7])

$$I = \frac{\Gamma_2^-\Gamma_1^+ - \Gamma_2^+\Gamma_1^-}{\Gamma_1^+ + \Gamma_2^+ + \Gamma_1^- + \Gamma_2^-}\, e.$$

Assuming $|\gamma_i| \gg 1$, i.e., sufficiently low temperature T, we simplify the expression for the current, which finally reads

$$I = \frac{k_B T}{e}\frac{\gamma_1\gamma_2}{\gamma_1 R_2 + \gamma_2 R_1}\left[\exp\left(-|\gamma_1|\right) - \exp\left(-|\gamma_2|\right)\right].$$

The *dc* component $\langle I(\delta Q_0)\rangle$ of the SET current I is obtained by averaging this equation over the voltage $v = v_{\rm ac}\sin\omega t$ with the weight

$$P(v) = \frac{1}{\pi\sqrt{{v_{\rm ac}}^2 - v^2}}.$$

Notice that the weight function $P(v)$, which can be considered as a probability density to find a value of the voltage within the interval $(v, v + {\rm d}v)$, equals to the ratio of the time-interval ${\rm d}t = 2{\rm d}v/v_0\omega\cos\omega t$, when this event happens, to the period $2\pi/\omega$. The resulting dependence is shown by solid line in Fig.3. One can see a good agreement between the experimental data and theoretical fit.

The observed feature of an asymmetric SET transistor demonstrates that it can be used as a noise level sensor for the bias and signal lines of a measuring setup. For example, the sensitivity of the studied transistor to noise signal in the bias lines was roughly estimated as $20\,{\rm nV/Hz^{1/2}}$ in the frequency range from $\Delta f = 0.1 \div 10\,$kHz. The amplitude of the observed current peaks in our setup was about 0.1 pA, i.e. limited by resolution of the current preamplifier.

Moreover, the asymmetric SET transistor can also be used as a radio frequency driven electrometer operating in a linear regime. The maximum current-to-charge ratio of the device, $\eta = |d\delta I(Q_0 = 0)/d\delta Q_0|$, for given sample and $V_{\rm ac} = 20\,\mu$V (see Fig.3) is about $0.3\,{\rm nA}/e$. This value is of the same order as that of typical SET electrometers. For example, in the traditional regime of the same amplitude of *dc* bias ($V_{\rm dc} = 20\,\mu$V) this electrometer has slightly better value of η, i.e. 0.7 nA/e at $I = 8\,$pA (see Fig. 4). The current-to-charge ratio η can also be found from analytical expression for $\langle I(\delta Q_0)\rangle$ as corresponding derivative $\langle(\partial I(\delta Q_0)/\partial\delta Q_0)_{\delta Q_0=0}\rangle$. The analytical expression for this average is rather cumbersome, but easy for numerical calculations. In this way we found the current-to-charge ratio numerically as a function of T and the dimensionless parameter of asymmetry C_2/C_Σ. Figure 5 shows the dependence of η on the value of C_2/C_Σ calculated for several values of the transistor

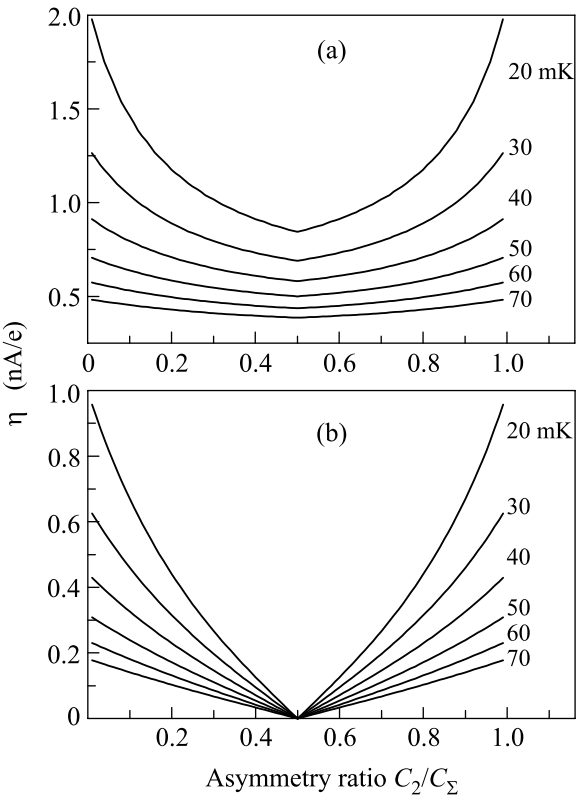

Fig.5. The current-to-charge transfer coefficient η in SET transistor versus asymmetry ratio at different temperatures. $V_{\rm ac} = V_{\rm dc} = 20\,\mu$V. (a) – *dc* regime; (b) – *ac* regime

temperature in *ac* and *dc* regimes. Lower current-to-charge ratio in *ac* regime can be understood from the fact that the effective action of *ac* signal on η is more than two times weaker than the action of *dc* signal of the same amplitude.

In some experimental situations (for example, RF-SET sensor) the zero bias regime with *ac* or *noise* pumping can be considered as more convenient for SET transistor operating as electrometer. Such a regime of the electrometer operation has presumably weak back action on the background charges located in dielectric around the island [8] and, therefore, the device is less subject to the drift of the offset charge bias.

3. Summary. In this paper we explored a rather delicate regime ($V \ll e/C_\Sigma$) of the transistor operation which is important for unperturbed measurements. The obtained results demonstrate the remarkable nonlinear characteristics of the strongly asymmetric SET transistor which can operate either as a linear electrometer or as a sensitive nonlinear noise detector useful for characterization of an experimental setup. Further investigations of such SET transistors in different regimes and especially their noise characteristics are clearly needed. The available technology makes it possible to fabricate these transistors with very high degree of asymmetry.

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